

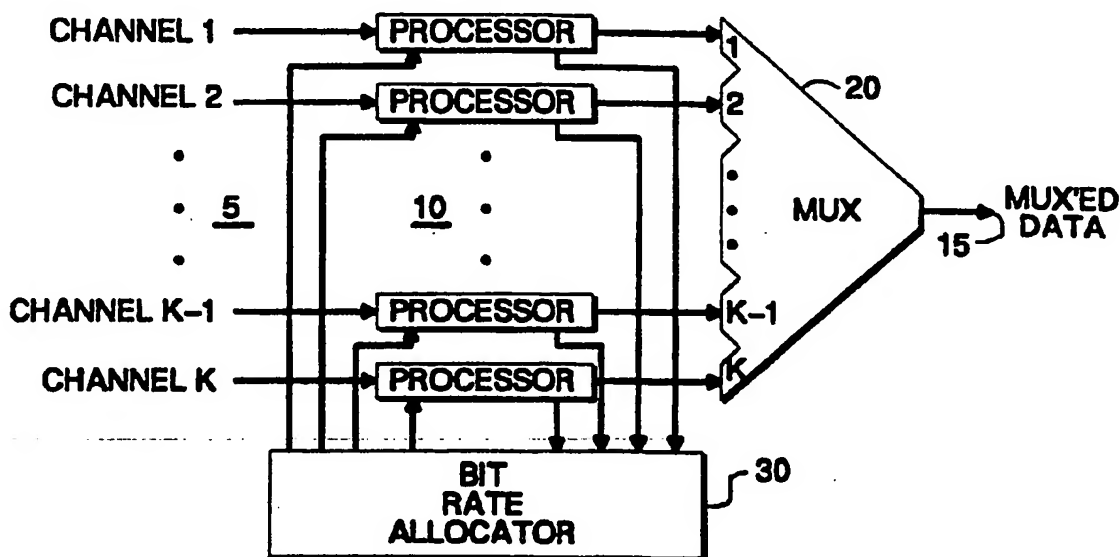


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(54) Title: A SYSTEM FOR DYNAMICALLY ALLOCATING A SCARCE RESOURCE



(57) Abstract

A system for dynamically allocating a resource is disclosed which includes a plurality of resource users (5) and a resource (15, 20) having a maximum utilization level sharable among the plurality of resource users (5). A plurality of need analyzers (10, 16), associated with respective resource users (5), dynamically generate respective signals (COMPLEXITY), each representing the relative need for the resource (15, 20) by the associated resource user (5). A plurality of access controllers (10, 14), associated with respective resource users (5), control access to the resource (15, 20) by the associated user (5) in response to an allocation signal (CONTROL). A resource allocator (30) dynamically generates allocation signals (CONTROL), representing allocated resource utilization levels for associated users (5), in response to the plurality of need representative signals (COMPLEXITY) from the need analyzers (10, 16).

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A SYSTEM FOR DYNAMICALLY ALLOCATING A SCARCE RESOURCE

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The present invention is related to a system for dynamically allocating a scarce resource among several competing users in response to indications of need from the users.

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BACKGROUND OF THE INVENTION

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It is often necessary for a scarce resource to be shared among several users. For example, a plurality of video signals from respective sources, which may be television network feeds, television stations, or other video sources, may be combined and transmitted over a satellite link for broadcast to respective television receivers in consumers' homes. An exemplary satellite link includes a digital transmission path capable of transmitting 24 megabits per second (Mbps). In order to maximize efficiency and utilization of such a link, it is necessary for several video signals to share the link. For example, it may be desired to share the above satellite transmission link among at least six video signal channels. In this case, the scarce resource is the bandwidth, or bit rate, in the satellite transmission link. This resource is shared in the transmission system by allocating some portion of the bandwidth or bit rate of the transmission link to each of the video signals.

30

35

One known method for performing the multiplexing function uses constant bit rate (CBR) encoders for each channel. In such a system, the video signal from each channel is supplied to a CBR encoder. A CBR encoder produces a digitally encoded bit stream, representing the video signal supplied to it, at a predetermined constant bit rate. To produce a constant bit rate signal, a CBR encoder continually modifies the number of quantizing levels into which the video signal is encoded. Using fewer quantizing levels requires fewer bits to represent those levels, and the overall

number of bits required to represent the video signal is reduced.

- 5 Conversely, using more quantizing levels requires more bits to represent those levels, and the overall number of bits required to represent the image is increased.

10 However, varying the quantization levels in an encoded signal representing an image effects a corresponding change in the quality of the image reproduced from the encoded signal. Using fewer quantization levels results in a lower quality reproduced image than using more quantization levels. Thus, in a CBR encoder, video signals representing spatially and/or temporally more complex images are encoded in such a manner that the
15 quality of the reproduced image is lower than that of less complex images.

20 Because CBR encoders produce a constant bit rate, controlling the multiplexing of video signals from a plurality of such encoders is simplified. Each encoder is *a priori* allocated a bit rate representing its quota of the total available bit rate of the transmission link. One known allocation method allocates equal portions of the total bit rate of the transmission link to each encoder. However, video signals representing different program types inherently have differing complexities. For example, a
25 video channel transmitting a basketball game has a much higher complexity than one transmitting a panel discussion. Thus, the quality of the image reproduced from the encoded video signal representing the basketball game will be lower (probably substantially lower) than that of the panel discussion.

30 Another known allocation method, which attempts to solve this problem, *a priori* allocates different bit rates to each CBR encoder based on the expected image complexity of the signal to be encoded. Thus, the channel transmitting a basketball game would be allocated a larger proportion of the total bit rate of the
35 transmission link than the channel transmitting the panel discussion. Such an allocation method can result in the quality of

the images reproduced from the encoded signals representing
5 both the basketball game and the panel discussion being more
nearly equal.

Yet another known allocation method allocates the
proportion of the total bit rate of the transmission link to channels
based on payment by the provider of the signal. The more the
10 provider pays for the transmission of the channel, the greater the
proportion of the total bit rate of the transmission link allocated to
that channel, and the better the quality of the image reproduced
from the encoded signal through that channel.

15 BRIEF SUMMARY OF THE INVENTION

The inventor has realized, however, that the complexity of a
video signal cannot always be specified *a priori*. For example, a
news broadcast contains scenes of very low complexity, (e.g. a
20 news reader sitting behind a desk reading news) interspersed
with scenes of very high complexity (e.g. a video clip of a
basketball game). If such a video channel were *a priori* allocated
a high proportion of the total bit rate of the transmission link,
then the basketball game scene would be reproduced with
25 acceptable quality, but the news reader scene would be encoded
with too high a quality, or, in other words, using more bits than
are necessary. On the other hand, if such a video channel were
allocated a lower proportion of the total bit rate of the
transmission link, then the news reader scene would be
30 reproduced with acceptable quality using a reasonable number of
bits, but the allocated bit rate would be insufficient to reproduce
the basketball game scene with acceptable quality.

The inventor further realized that each video source, on the
average, may be characterized in the same manner as the above
35 news broadcast. I.e. almost every video signal of commercial
interest contains scenes of high complexity interspersed with

5 scenes of low complexity. He also realized that the scenes of
differing complexity are uncorrelated in time. Furthermore, he
has found that, within any given frame period, the images of the
different channels have differing complexities, and that these
complexity variations are also uncorrelated in time.

10 It was found desirable that the scarce resource of
transmission link bit rate be dynamically allocated based on a
measure of need by each user. In the above example, it is
desirable that bit rates be dynamically allocated to different
channels based on the current image complexity of those channels.
15 The complexity of the images currently being transmitted for all
the channels are evaluated, and a proportion of the total bit rate
of the transmission link is allocated to each channel corresponding
in some manner to the relationship of the complexity of the
current image of that channel to the overall complexity of the
images of all the channels.

20 In accordance with principles of the present invention, a
system for dynamically allocating a resource includes a plurality
of resource users and a resource having a maximum utilization
level sharable among the plurality of resource users. A plurality
of need analyzers, associated with respective resource users,
25 dynamically generate respective signals, each representing the
relative need for the resource by the associated resource user. A
plurality of access controllers, associated with respective resource
users, control access to the resource by the associated user in
response to an allocation signal. A resource allocator dynamically
30 generates allocation signals, representing allocated resource
utilization levels for associated users, in response to the plurality
of need-representative signals from the need analyzers.

BRIEF DESCRIPTION OF THE DRAWING

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Fig. 1 is a block diagram of a multiplexer system according to the present invention;

Fig. 2 is a block diagram of a channel processor which may be used in the multiplexer system illustrated in Fig. 1;

10 Fig. 3 is a block diagram of a portion of an MPEG encoder which may be used in the channel processor illustrated in Fig. 2;

Fig. 4 is a block diagram of a bit rate allocator which may be used in the multiplexer system illustrated in Fig. 1;

15 Fig. 5 is a more detailed block diagram of a regulator which may be used in the MPEG encoder illustrated in FIG. 3; and

Figs 6, 7 and 8 are timing diagrams illustrating sampling of complexity information.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

20

Fig. 1 is a block diagram of a multiplexer system incorporating the present invention. In Fig. 1, all signal paths are illustrated as single signal lines. However, one skilled in the art will understand that the illustrated signal paths could carry
25 multibit digital signals, either in parallel, in which case the signal paths would be composed of multiple signal lines, or serially, in which case the signal paths could be a single data line and/or include a data and clock signal line. Other control and clock signal paths, not germane to the understanding of the present invention
30 have been omitted from the figure to simplify it.

In Fig. 1 a plurality of input terminals 5 are coupled to sources (not shown) of video signals (CHANNEL 1 - CHANNEL K) which are to be transmitted together over a data link. The plurality of input terminals 5 are coupled to respective data input
35 terminals of a corresponding plurality of channel processors 10. Respective data output terminals of the plurality of channel

processors 10 are coupled to corresponding data input terminals 1
5 - K of a multiplexer (MUX) 20. A data output terminal of
multiplexer 20 is coupled to an output terminal 15 of the
multiplexer system. Output terminal 15 is coupled to utilization
circuitry (not shown) for transmitting the multiplexed data stream
(MUX'ED DATA) over the transmission link.

10 Each of the plurality of channel processors 10 further
includes a complexity output terminal and a control input
terminal. The respective complexity output terminals of each of
the plurality of channel processors are coupled to corresponding
15 complexity input terminals of a bit rate allocator 30, and
respective quota output terminals of the bit rate allocator 30 are
coupled to the corresponding control input terminals of the
plurality of channel processors 10.

In operation, each channel processor receives a signal at its
control input terminal representing the bit rate allocated to it for
20 the next quota period. The channel processor then encodes the
signal at its data input terminal for the next quota period into a
digitally encoded signal at the allocated bit rate. The encoded
data signal is supplied to the corresponding input terminal of
multiplexer 20. Multiplexer 20 operates in a known manner to
25 combine the signals from all the channel processors into a
multiplexed data stream. The multiplexed data stream is then
supplied to the circuitry comprising the data link for transmission,
also in a known manner.

During the encoding process, the channel processor 10
30 generates a signal at its complexity output terminal representing
the coding complexity of the signal being encoded. The bit rate
allocator 30 receives the signals from the complexity output
terminals of the channel processors 10, and, based on all of the
complexity signals, dynamically adjusts the bit rate quotas for the
35 next quota period among the plurality of channel processors 10.
In a preferred embodiment, more complex signals are

5 dynamically allocated a relatively higher bit rate than less complex signals. Different methods of determining the complexity of the video signal and for allocating bit rates based on the complexities are described below.

10 Fig. 2 is a block diagram of a channel processor which may be used in the multiplexer system illustrated in Fig. 1. In Fig. 2, elements similar to those in Fig. 1 are designated by the same reference number, and are not described in detail below. In Fig. 2, a data input terminal 5 is coupled a video signal source (not shown). Data input terminal 5 is coupled to a data input terminal of a constant bit rate encoder (CBR) 14, and a complexity analyzer 15 16. A data output terminal of the CBR encoder 14 is coupled to an input terminal of multiplexer (MUX) 20 (of Fig. 1). A control input terminal (CONTROL) of the channel processor 10 is coupled to a quota input terminal Q of the CBR encoder 10. An output terminal of the complexity analyzer 16 is coupled to the complexity output 20 terminal (COMPLEXITY) of the channel processor 10.

In operation, the complexity analyzer 16 analyzes the complexity of the video signal at the data input terminal 5. A signal is produced at the output terminal of the complexity analyzer 16 representative of the complexity of the input signal. 25 The complexity representative signal is supplied to the bit rate allocator 30 (of Fig. 1). In response to this complexity signal (and those of the other channel processors 10), bit rate allocator 30 provides a signal to the control input terminal (CONTROL) of this channel processor 10 (and the other channel processors 10) 30 representing the bit rate allocated to this channel processor 10. The CBR encoder 14 provides a data path between its data input and data output terminals for producing an output signal encoded at a constant bit rate. The constant bit rate is set in response to the signal at the quota input terminal Q from the control input 35 terminal (CONTROL) of the channel processor 10 from the bit rate allocator 30.

It is possible that circuitry in the CBR encoder 14 can also be
5 utilized by the complexity analyzer 16 in performing its analysis.
In such a case, data is supplied from within the CBR encoder 14
directly to the complexity analyzer 16, as illustrated in phantom
in Fig. 2. Such data from the CBR encoder 14 may supplement
data from the input terminal 5, or replace it altogether, in which
10 case there is no direct connection of the complexity analyzer to
the data input terminal 5.

In a preferred embodiment, each CBR encoder 14 is an
encoder which compresses and encodes a video signal in
accordance with a standard promulgated by the Moving Picture
15 Expert Group (MPEG), termed an MPEG encoder. Fig. 3 is a block
diagram illustrating a portion of an MPEG encoder 14. The known
components of the MPEG encoder 14 will not be described in
detail below. MPEG encoders include other elements, not germane
to an understanding of the present invention, which have been
20 omitted from the figure to simplify it.

In Fig. 3, a data input terminal 5 (DATA IN) of MPEG
encoder 14 is coupled to a source (not shown) of a video signal to
be compressed and encoded. Input terminal 5 is coupled to an
input terminal of a frame buffer 41. Frame buffer 41 includes a
25 plurality of frame period buffers or delay lines and a plurality of
output terminals producing respective signals representing
portions of different, but temporally adjacent, frames or pictures.
The plurality of output terminals of the frame buffer 41 are
coupled to corresponding input terminals of a motion estimator
30 42. An output terminal of the motion estimator is coupled to a
discrete cosine transform (DCT) circuit 43. An output terminal of
DCT circuit 43 is coupled to a data input terminal of a variable
quantizer (Qu) circuit 46. An output terminal of variable
quantizer circuit 46 is coupled to an input terminal of a variable
35 length coder (VLC) 47. An output terminal of VLC 47 is coupled to
an input terminal of an output buffer 48. A data output terminal

of output buffer 48 is coupled to a data output terminal (DATA
5 OUT) of MPEG encoder 14. Data output terminal (DATA OUT) of
MPEG encoder 14 is coupled to a corresponding input terminal of
multiplexer 20 (of Fig. 1).

A status output terminal of output buffer 48 is coupled to a
status input terminal of a bit rate regulator 49. A control output
10 terminal of bit rate regulator 49 is coupled to a control input
terminal of variable quantizer 46. A quota input terminal Q of
MPEG encoder 14 is coupled to a corresponding quota output
terminal of bit rate allocator 30. The quota input terminal Q of
the MPEG encoder 14 is coupled to a control input terminal of
15 regulator 49.

In operation, MPEG encoder 14 operates in a known manner
to compress and encode the video signal at its input terminal for
the next quota period at a bit rate determined by the signal at its
Q input terminal. In the following example, an MPEG encoder
20 encoding a video signal partitioned into groups (GOPs) consisting
of twelve pictures or frames is described. However, it should be
understood that the number of pictures or frames in a GOP can
vary. Also in the following example, it is assumed that the bit
rate allocation for each MPEG encoder is updated once each GOP,
25, i.e. the quota period is the GOP period. However, it should also be
understood that the quota period may be different, and may even
vary over time.

The frame buffer 41 receives and stores data representing
the portion of the twelve frames in the exemplary GOP currently
30 being encoded necessary to perform motion estimation, in a
manner described below. This data is supplied to motion
estimator 42. In the preferred embodiment, the first one of the
twelve frames or pictures is used as a reference frame (I frame),
and is passed through the motion estimator to DCT circuit 43. For
35 the remainder of the frames, a motion vector is generated in
motion estimator 42 for each one of a plurality of 16 pixel by 16

line blocks in each picture or frame, termed macroblocks in the
5 MPEG standard document, either from preceding frames alone (P
frames), or interpolated from both preceding and succeeding
frames (B frames). As described above, frame buffer 41 holds the
data necessary for the motion estimator to perform the estimation
10 from preceding frames or the interpolation from preceding and
succeeding frames. The generated motion vectors for a particular
frame are then compared to the actual data in the frame being
estimated and a motion difference signal is generated, and
supplied to DCT circuit 43.

In the DCT circuit 43, the 16 pixel by 16 line macroblocks of
15 spatial data from the I frame and motion difference signals from
the P frames and B frames are divided into six 8 pixel by 8 line
blocks (four luminance blocks, and two subsampled chrominance
blocks) termed microblocks in the remainder of this application, in
accordance with the MPEG standard document. A discrete cosine
20 transform is performed on each microblock. The resulting 8 by 8
blocks of DCT coefficients are then supplied to variable quantizer
46. The 8 by 8 blocks of coefficients are quantized, scanned in a
zig-zag order and supplied to VLC 47. The quantized DCT
coefficients, and other side information (related to parameters of
25 the encoded GOP), representing the GOP are encoded using run-
length coding in the VLC 47, and supplied to output buffer 48.

It is known that the most direct way to control the output
bit rate of VLC 47, and thus maintain the allocated constant bit
rate for the MPEG encoder 14, is to control the number of
30 quantizing levels (or, put another way, the quantizing step size) to
be used for quantizing each block of DCT coefficients in the
variable-quantizer 46. The control signal supplied to the variable
quantizer 46 from the bit rate regulator 49 performs this
controlling function. Within a quota period, which is the period
35 between successive bit rate quota update signals from the bit rate
allocator 30 (of Fig. 1), the bit rate regulator 49, in known manner,

5 supplies a control signal to the variable quantizer 46 which varies the number of levels into which each 16 by 16 macroblock in the GOP is being quantized in order to maintain the allocated bit rate for that quota period. The bit rate allocation for the bit rate regulator 49 in the present example is varied for each GOP period in response to the coding complexity values of the video signals in
10 each of the plurality of channels, in a manner described below.

In a preferred embodiment, bit rate allocator 30 (of Fig. 1), is a computer system having connections coupled to various circuit components in the plurality 10 of channel processors. Fig. 4 is a block diagram of the hardware forming the bit rate allocator
15 30. In Fig. 4, a microprocessor (μ P) 31 is coupled to a read/write memory (RAM) 32, a read-only memory (ROM) 33 and an input/output (I/O) controller 34 over a computer system bus 35. There are other components of the computer system, such as mass storage devices, and user terminals, which have not been
20 illustrated in order to simplify the figure. The I/O controller 34 has a plurality of input terminals (COMPLEXITY) coupled to corresponding complexity output terminals of the plurality 10 of channel processors (of Fig. 1) and a plurality of output terminals (QUOTA) coupled to corresponding quota input terminals of the
25 plurality 10 of channel processors.

The microprocessor 31, RAM 32, ROM 33 and I/O controller 34 operate as a computer system in known manner to execute programs stored in the ROM 33, store and retrieve data in the RAM 32 and receive data from and transmit data to the devices
30 attached to the I/O controller 34. The data representing the current coding complexity of the video signals being encoded in the plurality 10 of channel processors (of Fig. 1) are received from the corresponding output terminals of those channel processors at the I/O controller 34 via the COMPLEXITY input terminals in a
35 manner described below. The microprocessor 31 is notified of the receipt of this data in a known manner, e.g. polling, interrupt, etc.

The microprocessor 31 retrieves those signals from the I/O controller 34 via the computer system bus 35, determines the quota of bits for the next quota period for each of the encoders, and supplies signals representing those quotas to the plurality 10 of channel processors via the QUOTA output terminals at the next quota period.

10 A preferred method for determining the coding complexity of a video signal being encoded by an MPEG encoder 14 (of Fig. 3) utilizes the quantization scale factor (designated Q_{MB}) for each 16 by 16 macroblock and the number of bits (designated T_{MB}) used to encode that macroblock, for all the macroblocks in each picture or frame of the GOP. Fig. 5 is a block diagram of bit rate regulator 15 49 of the MPEG encoder 14 (of Fig. 3) and the complexity analyzer 16 (of Fig. 2) which generates a coding complexity representative signal according to this method. Various clock and control signals have been omitted from Fig 5, to simplify it. However, what 20 signals are required, and the necessary timing and voltage characteristics of these signals are well understood.

The complexity analyzer 16 illustrated in Fig. 5 is an example of a complexity analyzer utilizing information from the CBR encoder 14 only, as illustrated in phantom in Fig. 2. In Fig. 5, 25 bit rate regulator 49 has a status input terminal T_{MB} coupled to the status output terminal of output buffer 48 (of Fig. 3). The control output terminal Q_{MB} of bit rate regulator 49 is coupled to the control input terminal of variable quantizer 46 (of Fig. 3). Regulator 49 further has a control input terminal (Q) coupled to a 30 corresponding quota output terminal of the bit rate allocator 30 (of Fig. 1).

The status input terminal T_{MB} of the bit rate regulator 49 is also coupled to a first input terminal of a first adder 92. An output terminal of the first adder 92 is coupled to an input 35 terminal of a first latch 93. An output terminal of the first latch 93 is coupled to a first input terminal of a multiplier 94 and a

second input terminal of the first adder 92. An output terminal of the multiplier 94 is coupled to an input terminal of a second latch 95. An output terminal of the second latch 95 is coupled to a coding complexity output terminal X_{pic} . Complexity output terminal X_{pic} is coupled a corresponding complexity input terminal of bit rate allocator 30 (of Fig. 1).

10 The control output terminal Q_{MB} of bit rate regulator 49 is also coupled to a first input terminal of a second adder 96. An output terminal of the second adder 96 is coupled to an input terminal of a third latch 97. An output terminal of the third latch 97 is coupled to a numerator input terminal N of a divider 98 and to a second input terminal of the second adder 96. An output terminal of divider 98 is coupled to a second input terminal of the multiplier 94. A register 99 has an output terminal coupled to the denominator input terminal D of the divider 98.

20 In operation, for each macroblock, bit rate regulator 49 generates a quantizing scale factor signal Q_{MB} for the variable quantizer 46, in a known manner, based on the current bit rate quota and the number of bits used to encode preceding pictures, and then receives a signal from the output buffer 48 indicating the number of bits T_{MB} used to encode that macroblock. The variable quantizer 46 (of Fig. 3) quantizes the DCT coefficients in each macroblock in accordance with the quantizing scale factor Q_{MB} . The quantizing scale factor Q_{MB} represents the quantizing step size, or percentage of the full dynamic range of the DCT coefficients in each quantizing level. A high value for Q_{MB} means 30 that there is a larger quantizing step size, and, consequently, fewer quantizing levels. Conversely, a low value for Q_{MB} means that there is a smaller quantizing step size, and, consequently, more quantizing levels. In the preferred embodiment, Q_{MB} is a five bit integer (having values between 1 and 31).

35 An average quantizing scale factor for all the macroblocks in a complete picture or frame (designated Q_{pic}) is then calculated as

follows. At the beginning of each frame or picture, latches 93 and
 5 97 are cleared to zero in response to a clear signal (not shown).
 The combination of the second adder 96 and the third latch 97
 operate as an accumulator to continually sum the macroblock
 quantizing scale factors Q_{MB} from the bit rate regulator 49. At the
 same time, the combination of the first adder 92 and the first
 10 latch 93 operate as an accumulator to continually sum the number
 of bits used thus far to encode the frame or picture.

After all of the macroblocks in a frame or picture (a number
 designated N_{MB}) have been processed, latch 97 contains the sum
 of all of the macroblock quantizing scale factors Q_{MB} produced by
 15 bit rate regulator 49, and latch 93 contains the sum of all the bits
 used to encode the picture or frame T_{pic} . The divider 98 produces
 the quotient of the sum of all the macroblock quantizing scale
 factors Q_{MB} in the picture or frame, divided by the number of
 macroblocks in the picture or frame N_{MB} . This quotient is the
 20 average quantizing scale factor Q_{pic} for that frame or picture. The
 multiplier 94 produces the product of Q_{pic} and T_{pic} , which is the
 coding complexity for that picture (designated X_{pic}), i.e.
 $X_{pic} = T_{pic} \cdot Q_{pic}$. At the end of the picture or frame, the coding
 complexity signal X_{pic} is latched into the second latch 95 in
 25 response to a clock signal (not shown). The above described cycle
 then repeats for each frame or picture in the video signal being
 encoded.

The coding complexity X_{pic} is then supplied from latch 95 to
 a complexity input terminal of the I/O controller 34 of the bit rate
 30 allocator 30 (of Fig. 4) which performs the remaining processing to
 obtain the coding complexity for the GOP. The coding complexity
 for a GOP (designated X_{GOP}) is the sum of the X_{pic} 's for all of the
 pictures in that GOP. (See equation (1)). The μP 31 acts as an

$$\begin{aligned}
 35 \quad X_{GOP} = & \sum_{\text{all pics in GOP}} T_{pic} \cdot Q_{pic} = \sum_{\text{all pics in GOP}} X_{pic} \quad (1)
 \end{aligned}$$

accumulator by retrieving each X_{pic} value from the I/O controller
 5 34, and summing them over all of the frames or pictures in the
 GOP.

The number of frames or pictures in a GOP (designated N)
 generally remains constant. While N is constant, X_{GOP} can be
 calculated, on a sliding window basis, by adding the coding
 10 complexity value X_{pic} of the latest picture, and subtracting the
 coding complexity value from the oldest picture in the GOP. In
 this case, an updated value of X_{GOP} is available after each frame or
 picture. However, N can change. If N changes, then X_{GOP} for the
 newly defined GOP must be calculated by summing the coding
 15 complexity values X_{pic} from the new number of preceding
 pictures in the newly defined GOP, as in equation (1).

As described above, it is possible that different channels
 operate at different frame or picture rates, e.g. the standard video
 frame rate (in the U.S.) is 29.97 frames per second, for film images
 20 it is 24 frames per second, and for cartoons it is 15 frames per
 second. It is also possible that different channels have different
 numbers of pictures or frames in a GOP. Thus, it is possible that
 different channels have different GOP time periods. In order to
 accurately allocate bits to channels under such conditions, the GOP
 25 coding complexity values of the plurality of channels in such
 situations are time normalized in the bit rate allocator 30 by
 dividing the GOP complexity value from equation (1) for each
 channel by that channel's GOP time period (designated GOP_{time}).
 (See equation (2)). The normalized GOP coding complexity value

30

$$X_{norm_GOP} = \frac{X_{GOP}}{GOP_{time}} \quad (2)$$

(designated X_{norm_GOP}) is then used to allocate bits among the
 different channels. The timing of the sampling of the complexity

35

values, and the generation of quota values for such systems will be discussed in more detail below.

5 Referring back to Fig. 5, as described above, for each macroblock, bit rate regulator 49 generates a quantizing scale factor signal Q_{MB} for variable quantizer 46, and then receives a signal from the output buffer 48 indicating the number of bits T_{MB} used to encode that macroblock. These signals may
10 alternatively be supplied directly to the I/O controller 34 in the bit rate allocator 30 (of Fig. 4). The μP 31 may then calculate the appropriate coding complexity measure (from equation (1) or equations (1) and (2)) internally.

Furthermore, in order to simplify the transmission, the
15 coding complexity value for each picture X_{pic} may be scaled. In a preferred embodiment, this value is scaled, after multiplier 94, into an eight bit number. This scaled value is then passed to the bit rate allocator 30 (of Fig. 4). It may also be desirable for the computer system to maintain a file of the picture complexity
20 values X_{pic} , for example in a mass storage device (not shown), for other reasons, such as allowing recalculation of the coding complexity value in the event N changes. Storage of an hour of 8 bit X_{pic} values will take 108 kilobytes (kB) for standard video and 86 kB for film.

25 In the discussion below, X^i will represent the currently available appropriate one of either X_{GOP} (if all channels have the same GOP time period) or X_{norm_GOP} from the i^{th} channel processor. The bit rate allocator 30 (of Fig. 1) generates
30 respective quota (Q) signals representing allocations of the available bits in the transmission link for the next quota period based on the coding complexity values X^i from all of the K channel processors forming the plurality of channel processors 10. The predetermined transmission link bit rate from the output terminal of the multiplexer 20 (of Fig. 1) (designated R) is allocated among
35 the plurality 10 of channel processors, so that the i^{th} channel processor receives a bit rate allocation designated R^i .

One method for allocating bit rates in the transmission link
 5 to the different channels is a linear allocation based on the
 currently available coding complexity X^i of the preceding GOP
 period (on a sliding window basis, as discussed above) for all of
 the plurality 10 of channel processors (of Fig. 1). In this method,
 each processor i receives the same proportion R^i of the total bit
 10 capacity R as the coding complexity of that encoder X^i bears to the
 total coding complexity of all the encoders. (See equation (3)).

$$R^i = \frac{X^i}{\sum_{j=1}^K X^j} R \quad (3)$$

However, it has been found that there is a lower bit rate allocation
 below which the quality of a reproduced image drops
 precipitously. In addition, in the illustrated embodiment, the bit
 20 rate allocations for the next quota period depends upon the
 complexity measures from the preceding GOP. Thus, if there is a
 scene change from a simple image to a complex image, there may
 be insufficient bits allocated to encode the new, complex, scene
 because the allocation for the new scene was based on the
 25 preceding, simple, scene.

An alternative method for allocating bit rates in the
 transmission link to different channels guarantees a minimum bit
 rate allocation RG^i to each encoder i , and allocates the remaining
 bits linearly, as in equation (3). (See equation (4)). Each channel

$$R^i = RG^i + \frac{X^i}{\sum_{j=1}^K X^j} [R - \sum_{j=1}^K RG^j] \quad (4)$$

may have a different guaranteed minimum bit rate depending
 5 upon the anticipated overall complexity of the video transmitted
 through the channel and/or pricing of the channel to the
 providers of the video signals.

Yet another alternative method for allocating bits in the
 transmission link to different channels provides a weighting factor
 10 P^i for each encoder i and allocates bits proportionately according
 to the coding complexity values X^i , as weighted by the weighting
 factors P^i . (See equation (5)). As in the guaranteed minimum
 allocation method of equation (4), the weighting factors P^i may
 15 depend on anticipated overall complexity of the video signal
 transmitted through the channel and/or pricing of the channel to
 the provider of the video signals.

$$R^i = \frac{P^i X^i}{\sum_{j=1}^K P^j X^j} (R) \quad (5)$$

20

A preferred method for allocating bits in the transmission
 link to different channels is a combination of the weighted
 allocation method of equation (5) and the guaranteed minimum
 25 allocation method of equation (4). In this method each channel is
 guaranteed a minimum allocation, and the remaining bits are
 allocated on a weighted proportion basis. (See equation (6)). As

$$R^i = R_G^i + \frac{P^i X^i}{\sum_{j=1}^K P^j X^j} [R - \sum_{j=1}^K R_G^j] \quad (6)$$

30

above, both the guaranteed minimum allocation and the weighting
 35 factors may depend upon the anticipated overall complexity of the

5 video signal transmitted over the channel and/or pricing of the channel to the provider of the video signals.

It is possible to further refine the bit allocations R^i , in response to other parameters of the system. For example, it has been found that there is an upper bit rate allocation value above which no improvement in the quality of the reproduced image is visible. Thus, an allocation of bits in excess of this upper allocation value is wasteful of bits in the transmission link. Also, the operator of the transmission link may impose a maximum bit rate allocation R_{\max} (which can reflect the above upper bit rate allocation value) and/or a minimum bit rate allocation R_{\min} for each channel.

In addition, in order to minimize the potential for bit rate control oscillations and thus maximize bit rate control stability, there may be imposed a maximum increment of increase α and/or decrease β in the bit rate allocation from one quota period to the next for a channel. As above, the values of the upper bit rate allocation value, the maximum and minimum bit rate allocations, and maximum increments of increase and decrease, may be different for the different channels, and may depend on the anticipated overall complexity of the video signal to be transmitted through this channel and/or the pricing of the channel to the provider of the video signals. In addition, it is possible for the maximum and minimum increments of increase and decrease to vary dynamically according to the degree of emptiness or fullness of the buffers in the channel.

Furthermore, the allocated bit rates may be further refined in order to provide buffer management, e.g. to ensure that the output buffers of the CBR encoders 10 (of Fig. 1) and the input buffers of the corresponding receiver decoders (not shown) do not overflow or underflow. Explicit buffer management is not necessary if the encoder buffer size E is controlled as illustrated in inequality (7), where D is the fixed decoder buffer size. If the

$$E \leq D \frac{R_{min}}{R_{max}} \quad (7)$$

5

encoder buffer size is selected according to inequality (7), the bit rate allocation may vary from R_{min} to R_{max} without inducing overflow or underflow in either the encoder or decoder buffers. However, this method unduly limits the size of the encoder buffer, thus, unduly limiting the rate control flexibility.

10

An alternative buffer management scheme is adaptive and uses the current, instantaneous bit rates for buffer management, rather than the fixed parameters R_{min} and R_{max} . Because the decoder buffer size was selected to be able to process data transmitted at the highest rate, R_{max} , the bit rate allocation can always be increased (to the system maximum, R_{max}) without overflowing the decoder buffer. However, there is an instantaneous minimum bit rate which must be maintained in order to assure that the data already in the encoder buffer gets transmitted to the decoder buffer before its decode time. Thus, a minimum bit rate allocation to ensure that the decoder buffer does not underflow must be dynamically calculated.

15

20

In dynamically calculating this minimum bit rate allocation, when decreasing the bit rate allocation, both a newly determined encoder buffer size, and the amount of data already placed in the encoder buffer in some preceding amount of time must be taken into account. The newly determined encoder buffer size for frame n , designated E_n , is determined in accordance with equation (8) in

25

30

$$E_n = \Delta R_{new} = \frac{R_{new}}{R_{max}} D \quad (8)$$

which Δ is the system delay time, which a constant time delay between when a frame of video arrives at the encoder and when that frame is displayed at the decoder; D is the fixed decoder

buffer size; and R_{new} is the new proposed bit rate allocation. This
 5 buffer size ensures that in steady state at the new bit rate
 allocation, there will be no overflow or underflow in the encoder
 and decoder buffers.

However, as described above, if the newly proposed bit rate
 allocation has been decreased, then there is a transition period,
 10 equal to the system delay time Δ , in which there may be too many
 bits already in the encoder buffer to be transmitted successfully
 to the decoder at the new lower rate. One proposed method for
 refining the newly proposed bit rate allocation is first to examine
 the number of bits, designated e , actually placed into the encoder
 15 buffer (buffer fullness) for the number of preceding frames in the
 system delay time Δ , designated Γ . Then the maximum buffer
 fullness number for the preceding Γ frames (designated $e_{max} \Gamma$) is
 compared to the newly determined encoder buffer size E_n , from
 equation (8). The minimum reduced bit rate allocation $R_{reduced}$
 20 for channel i which guarantees that all the bits from the preceding
 Γ frames will be transmitted successfully to the receiver decoder,
 then, is given in equation (9).

$$R_{reduced}^i = \frac{e_{max} \Gamma}{\Delta} \quad (9)$$

25

If such limits are imposed in a multiplexer system, then
 after bit rate allocations have been calculated according to
 equations (3), (4), (5) or (6), those bit rate allocations are checked
 to determine whether they fall within the current upper and
 30 lower limits for that channel. First, the upper and lower limits for
 each channel i are determined. The upper limit bit rate allocation
 for any quota period k (designated $R_{upper}^i[k]$) is the minimum of:
 the maximum permissible increased allocation over the previous
 quota period $k-1$; and the maximum bit rate allocation limit. (See
 35 equation (10)). The lower limit bit allocation for any quota period

$$R_{upper}^i[k] = \min \{ R_{max}^i, (1 + \alpha) R^i[k-1] \} \quad (10)$$

5
k, $R_{lower}^i[k]$, is the maximum of: the minimum bit rate allocation limit; the minimum permissible decreased allocation over the previous quota period k-1 and the minimum reduced bit rate allocation from equation (9). (See equation (11)). Then
10 adjustments in the bit rate allocations for the channels are made.

$$R_{lower}^i[k] = \max \{ R_{min}^i, (1 - \beta) R^i[k-1], e_{max} \Gamma / \Delta \} \quad (11)$$

15 If the allocated bit rate for any channel exceeds either limiting value, the bit rate allocation for that channel is set to that limiting value, and the available remaining bit rate is reallocated among the other channels. For example, if the bit rate allocated to a channel i, as calculated in equation (3), (4), (5) or (6), is greater than the upper limit for that channel, as calculated in equation
20 (10), then the bit rate for channel i is set to that upper limit R_{upper}^i . If, conversely, the bit rate is less than the lower limit calculated in equation (11), then the bit rate is set to that lower limit R_{lower}^i . (See equation (12)).

$$25 \quad R^i[k] = \begin{cases} R_{lower}^i[k] & \text{if } R^i[k] < R_{lower}^i[k] \\ R_{upper}^i[k] & \text{if } R^i[k] > R_{upper}^i[k] \\ R^i[k] & \text{otherwise} \end{cases} \quad (12)$$

30 If any of the bit rate allocations are changed by the limiting operations of equations (10), (11) and (12), then the remaining available bit rate is reallocated among the non-limited channels in accordance with equation (3), (4), (5) or (6). Then these channels are again checked against the limits in equations (10), (11) and (12). This cycle is repeated until all bit rate allocations are
35 finalized. In the above embodiment, the coding complexity period

is the GOP period, determined picture by picture on a sliding
5 window basis, which is of sufficient duration that changes in bit
rate allocations in a channel from one quota period to the next
should generally be relatively small. Consequently, equations
(10), (11) and (12) should only rarely be invoked.

The timing of the coding complexity sampling and
10 generation of updated bit rate quotas based on the coding
complexities is complicated if the channels are operating with
different GOP time periods. There are two approaches which yield
accurate coding complexity sampling and bit rate quota allocation
in this situation. In the first approach, a constant quota period is
15 calculated in such a manner that each channel has an equal
number of quota periods in each GOP. In this approach, the
number of sample and quota periods per GOP may vary from
channel to channel, but, for any channel, the number of such
sample and quota periods within a GOP is constant. In the second
20 approach, a sample is taken, and new allocation generated
whenever any channel begins a new GOP, and the number of bits
allocated in the new quota is calculated taking into account the
length of the time period from the previous sample to the current
sample.

25 Fig. 7 is a timing diagram illustrating the sampling and
quota updates in a system using the first approach. In order to
simplify the drawing, only two channels are illustrated. In Fig. 7,
channel 1 is an example of a channel transmitting standard video
having a frame rate of 30 frames per second (in the U.S.). Channel
30 2 is an example of a channel transmitting a film having a frame
rate of 24 frames per second. Each of the channels is assumed to
have 12 frames per GOP. Channel 1, thus, starts a new GOP every
0.4 seconds, or 2.5 GOPs per second, while channel 2 starts a new
GOP every 0.5 seconds, or 2 GOPs per second. The sampling rate
35 selected is one sample every 0.1 seconds. Thus, in channel 1,
there are four sample and quota updates in every GOP, and in

channel 2 there are five sample and quota updates in every GOP.
5 The sampling times, t_s , are illustrated by vertical dashed lines. Because the time periods between samples Δt is constant (0.1 seconds), equations (3) through (12), above, may be used without any modification in calculating the bit rate allocations for the next sample period. These bit rate allocations may be accumulated and
10 used in the channel processors 10 (of Fig. 1) according to the known scheme termed the "token and leaky bucket" scheme.

Fig. 8 is a timing diagram illustrating the sampling of coding complexity values and quota updating in a system using the second approach, described above. The respective channels
15 illustrated in Fig. 8 are carrying the same signals as in Fig. 7. In Fig. 8, samples of the coding complexity values from all the channels are taken whenever any channel begins a new GOP. New allocations are generated based on the values of those samples, and the time period Δt since the last sample. These sample times
20 are illustrated in Fig. 8 as vertical dashed lines $t_1 - t_8$, where t_2 , t_3 , t_4 , t_6 and t_8 correspond to starts of GOPs in channel 1, and t_1 , t_3 , t_5 and t_7 correspond to starts of GOPs in channel 2. Although t_3 illustrates a sampling time corresponding to starts of GOPs in both channel 1 and 2, there is no requirement that such a time
25 occur.

At each sample time, the current coding complexity values (from the preceding GOP, available picture by picture on a sliding window basis) in all the channels are sampled. Equations (3) through (12) may be used to calculate the next bit rate quota
30 proportions, but in determining the actual number of bits available to be allocated, the amount of time Δt since the last sample—must be taken into account. In order to properly compensate for the different sample periods, the total available bit rate R in equations (3) through (12) is replaced with the
35 number of bits available for allocation, designated C , which is the product of the total available bit rate R and the sample period Δt ,

i.e. $C=R\Delta t$. The number of bits calculated by equations (3) through
5 (12) are then allocated to the respective channel processors 10 (of
Fig. 1) which, as above, use the "token and leaky bucket" scheme
to accumulate and use the allocated bits. Either of the above two
above approaches will accurately allocate bit rates to the
10 respective channel processors 10 when the video signals from the
different channels 5 have different GOP time periods.

The timing of the sampling of coding complexity values and
the generation of updated bit rate quotas for the different
channels may be simplified if all of the channels are operating at
the same frame rate, and have the same number of frames in a
15 GOP, i.e. all the channels have the same GOP time period, GOP_{time} .
Fig. 6 is a timing diagram illustrating coding complexity sample
and quota update timing in such a system. In Fig. 6, each
horizontal line corresponds to a respective channel 1 - K. The
short vertical lines extending upward from the horizontal lines
20 represent the time when coding of an I frame is begun for that
channel, which is considered to be the beginning of a GOP for that
channel. The time period for a GOP, GOP_{time} , is equal in all of the
channels, but, as can be seen, the beginning times of the GOPs for
the respective channels are different. In fact, it has been found
25 desirable to have different starting times for the GOPs for the
respective channels so that coding of I frames do not overlap.
This increases the complexity variations across the different
channels.

It has been found that so long as the same number of I
30 frames, P frames, and B frames are taken into account in
calculating the coding complexity value, it does not matter that
those frames come from different GOPs. Thus, as shown by the
solid lines extending across all the channel's time axes, a coding
complexity value sample may be taken simultaneously from all
35 the channels at any time within a GOP. Updates of the bit rate
quotas for all of the channels may then be generated from that

sample and transmitted back to the channel processors 10 (of Fig. 1).

The above multiplexer system has been described as a collocated system. However, the plurality 10 of channel processors could reside in remote locations from the bit rate allocator 30 and the multiplexer 20. In such a system, communication links would be established between the encoders and the bit rate allocator. In this case, some portion of the bits transmitted between the processors 10 and the multiplexer could be dedicated to transmission of complexity information from the processors.

What is claimed is:

5

1. A system for dynamically allocating a resource, comprising:

a plurality of resource users (5);

10 a resource (15,20) having a maximum utilization level sharable among the plurality of resource users (5);

a plurality of need analyzers (10,16), associated with respective resource users (5), for dynamically generating respective signals (COMPLEXITY), each representing the relative need for the resource by the associated resource user (5);

15 a plurality of access controllers (10,14), associated with respective resource users (5), for controlling access to the resource (15,20) by the associated user (5) in response to an allocation signal (CONTROL); and

20 a resource allocator (30), for dynamically generating respective allocation signals (CONTROL) representing allocated resource utilization levels, in response to the plurality of need representative signals (COMPLEXITY) from the need analyzers (10,16).

25 2. The resource allocation system of claim 1, wherein the resource allocator (30) generates respective allocation signals (CONTROL) such that a user (5) having a relatively higher need will receive a relatively higher allocation than a user (5) having a relatively lower need.

3. The resource allocation system of claim 2, wherein the
5 resource allocator (30) generates respective allocation signals
(CONTROL) such that a user (5) is allocated a proportion of the
maximum utilization level equal to the proportion of the need
represented by the need representative signal (COMPLEXITY)
associated with that user (5) to the combined need represented by
10 all the need representative signals (COMPLEXITY).

4. The resource allocation system of claim 2, wherein:
each user (5) is assigned a respective predetermined
minimum resource utilization level; and
15 the resource allocator (30) generates respective allocation
signals (CONTROL) such that a user (5) is allocated its assigned
predetermined minimum resource utilization level, and further
allocated a proportion of a remaining resource utilization level, the
remaining resource utilization level being equal to the maximum
20 resource utilization level less the previously allocated
predetermined minimum resource utilization levels, the further
allocated proportion being equal to the proportion of the need
represented by the need representative signal (COMPLEXITY)
associated with that user (5) to the combined need represented by
25 all the need representative signals (COMPLEXITY).

5 5. The resource allocation system of claim 2, wherein:
each user (5) is assigned a respective predetermined
weighting factor; and

 the resource allocator (30) generates respective allocation
signals (CONTROL) such that a user (5) is allocated a proportion of
the maximum resource utilization level equal to the proportion of
10 the need represented by the need representative signal
(COMPLEXITY) associated with this user (5) to the combined need
represented by all the need representative signals (COMPLEXITY),
weighted by the predetermined weighting factor assigned to the
associated user (5).

15

 6. The resource allocation system of claim 2, wherein:
each user (5) is assigned a respective predetermined
minimum resource utilization level and a predetermined
weighting factor; and
20 the resource allocator (30) generates respective allocation
signals (CONTROL) such that a user (5) is allocated its assigned
predetermined minimum resource utilization level, and further
allocated a proportion of a remaining resource utilization level, the
remaining resource utilization level being equal to the maximum
25 resource utilization level less the previously allocated
predetermined minimum resource utilization levels, the further
allocated proportion being equal to the proportion of the need
represented by the need representative signal (COMPLEXITY)
associated with this user (5) to the combined need represented by
30 all the need representative signals (COMPLEXITY), weighted by
the predetermined weighting factor assigned to the associated
user (5).

7. The resource allocation system of claim 2, wherein:
5 each user (5) is assigned a respective predetermined resource utilization level allocation limit; and
the resource allocator (30), after generating respective resource utilization allocation signals (CONTROL), compares the respective resource utilization level allocations to the respective
10 predetermined resource utilization level allocation limits, and if a resource utilization level allocation exceeds an assigned predetermined resource utilization level allocation limit, generates an allocation signal (CONTROL) representing the predetermined resource utilization level allocation limit, instead of the previously
15 generated resource utilization level allocation for the respective user.

8. The resource allocation system of claim 7, where the predetermined resource utilization level allocation limit is a
20 maximum resource utilization level allocation.

9. The resource allocation system of claim 7, where the predetermined resource utilization level allocation limit is a
25 minimum resource utilization level allocation.

10. The resource allocation system of claim 2, wherein:
each user (5) is assigned a respective predetermined resource utilization level allocation increment limit; and
the resource allocator (30), after generating respective
30 allocation signals (CONTROL), compares the respective resource utilization level allocations to corresponding resource utilization level allocations represented by immediately preceding respective allocation signals (CONTROL) to determine respective resource utilization level allocation increments, and if a resource utilization
35 level allocation increment exceeds an assigned predetermined resource utilization level allocation increment limit, generates a

allocation signal (CONTROL) representing the resource utilization
5 level allocation represented by immediately preceding respective
allocation signal changed by the predetermined resource
utilization level allocation increment limit, instead of the
previously generated resource utilization level allocation for the
respective user.

10

11. The resource allocation system of claim 10, wherein
the predetermined resource utilization level allocation increment
limit is a maximum increment of increase of resource utilization
level.

15

12. The resource allocation system of claim 10, wherein
the predetermined resource utilization level allocation increment
limit is a maximum increment of decrease of resource utilization
level.

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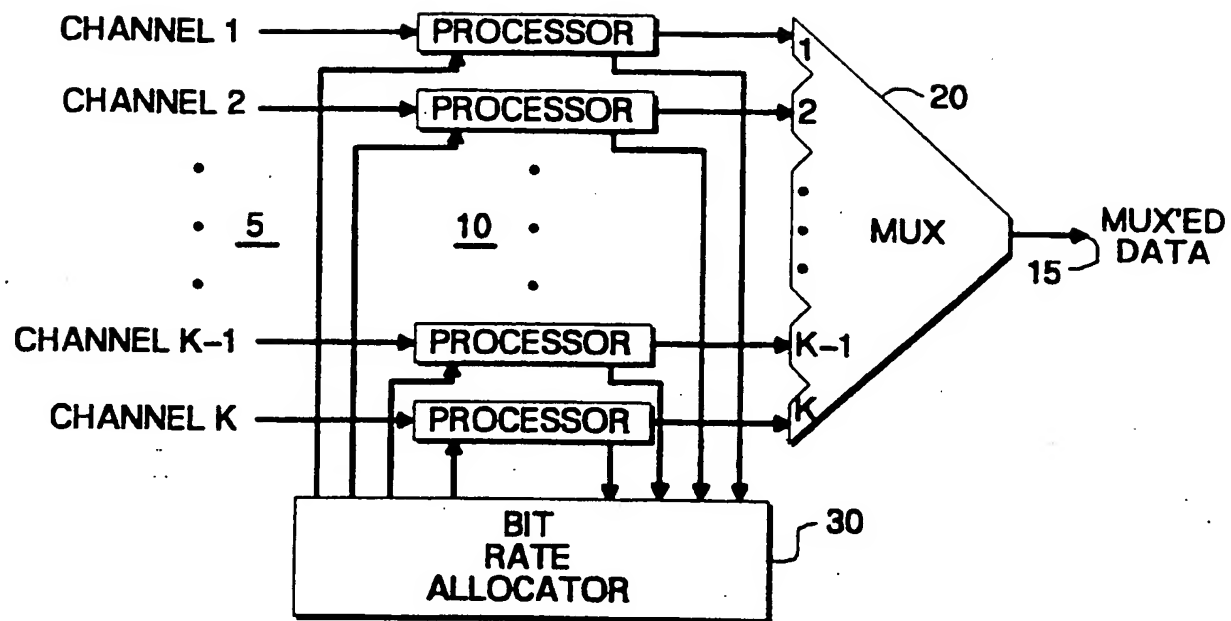


FIG. 1

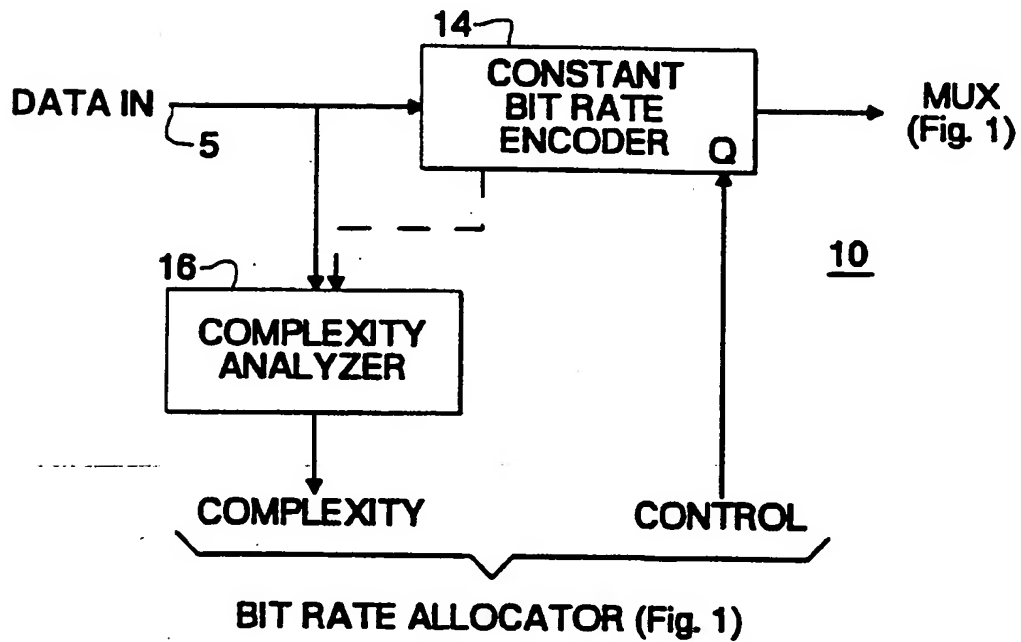


FIG. 2

2 / 3

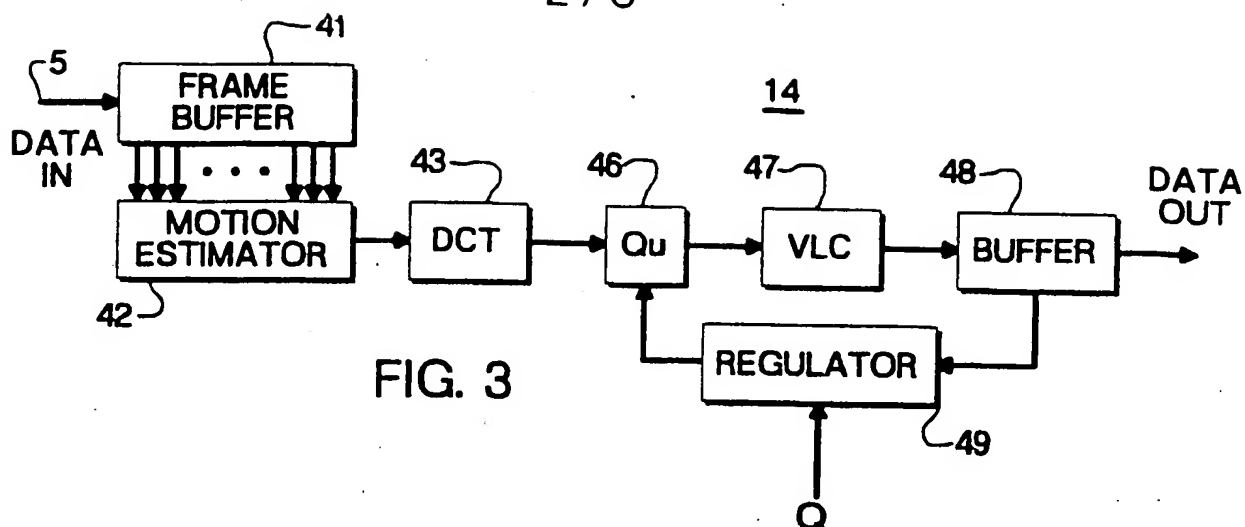


FIG. 3

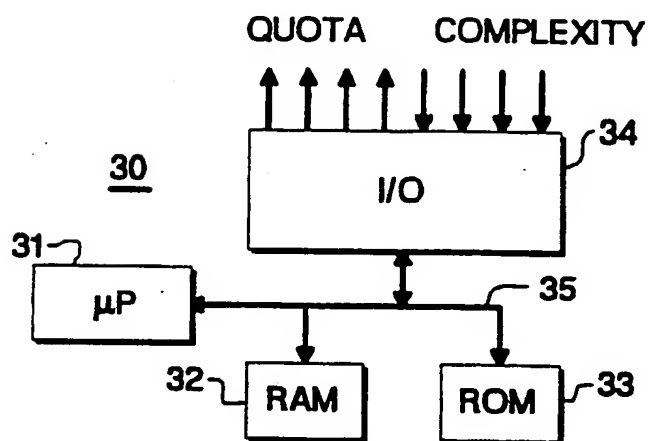


FIG. 4

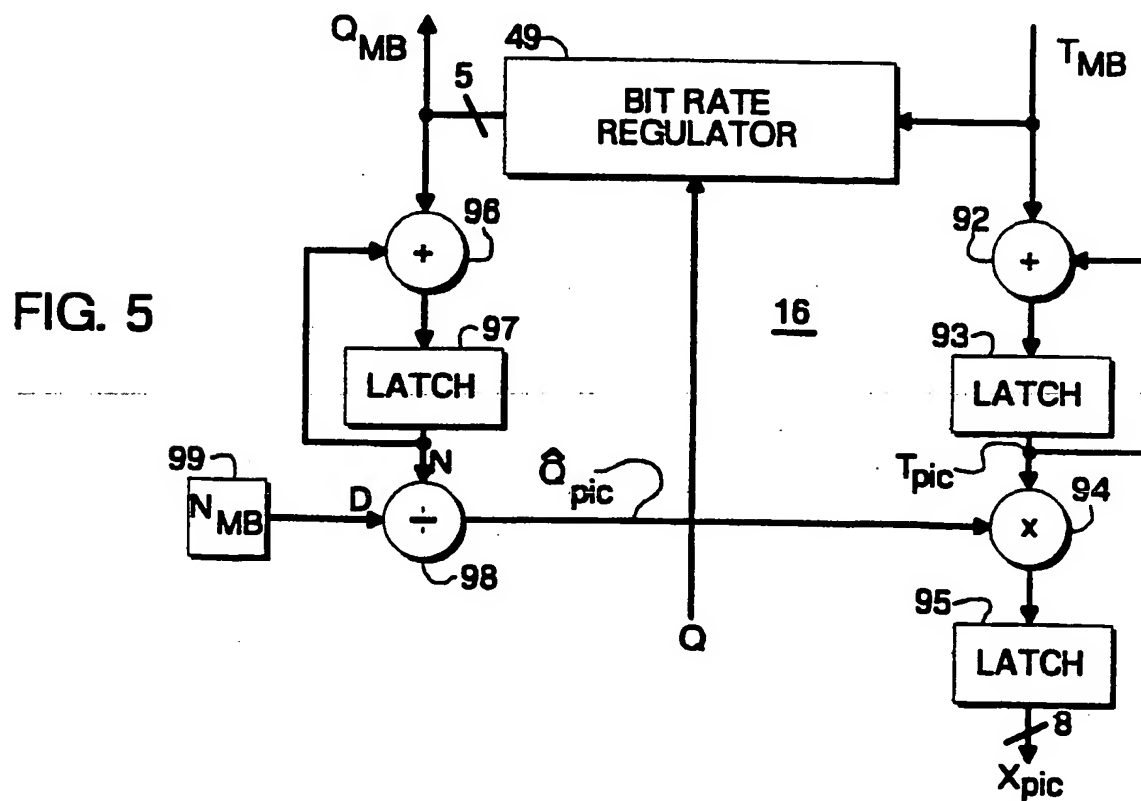


FIG. 5

3 / 3

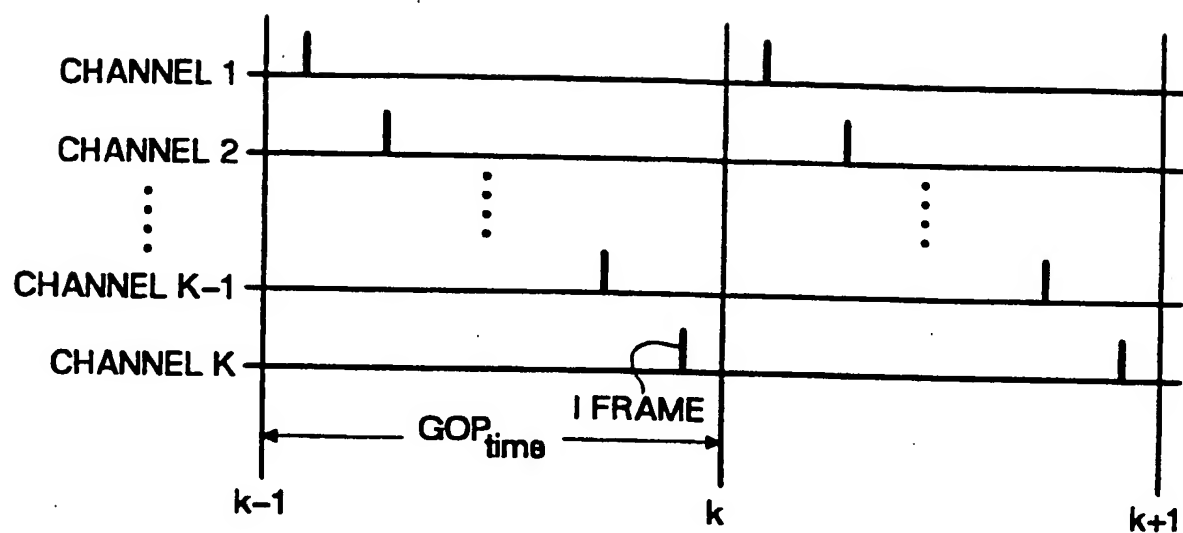


FIG. 6

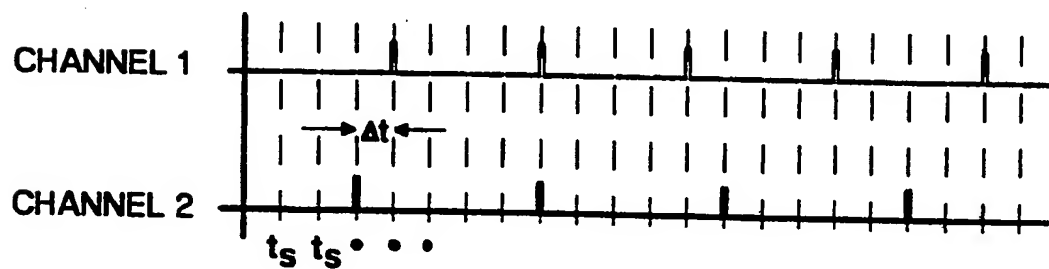


FIG. 7

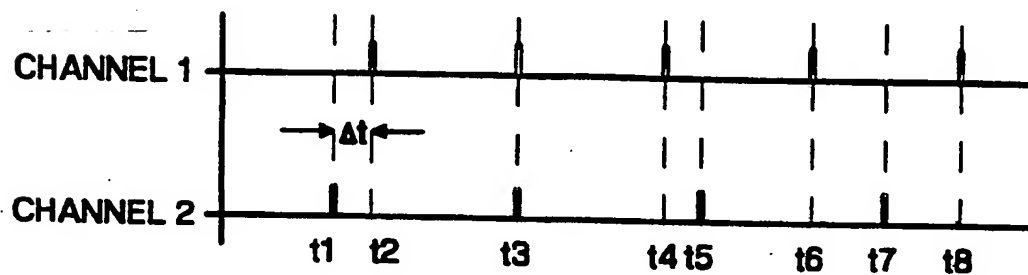


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/04421**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(5) :H04J 3/16, 3/22; H04N 7/12

US CL :Please See Extra Sheet.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : Please See Extra Sheet.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data: base consulted during the international search (name of data base and, where practicable, search terms used)

APS: CHANNEL#, ACCESS, CONTROL?, (RESOURCE OR BIT RATE OR BANDWIDTH)(P)ALLOCAT?, COMPLEXITY, UTILIZATION LEVEL, WEIGHTING FACTOR

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 5,115,309 (HANG) 19 May 1992, col. 4, line 24 to col. 5, line 27, fig.1	1-6
A	US, A, 4,713,776 (ARASEKI) 15 December 1987, see entire document	1-12
A	US, A, 5,134,476 (ARAVIND et al.) 28 July 1992, see entire document	1-12
A,P	US, A, 5,309,232 (HARTUNG et al.) 03 May 1994, see entire document	1-12

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	* T	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
* A* document defining the general state of the art which is not considered to be part of particular relevance	* X	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
* E* earlier document published on or after the international filing date	* Y	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
* L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	* &	document member of the same patent family
* O* document referring to an oral disclosure, use, exhibition or other means		
* P* document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

22 OCTOBER 1994

Date of mailing of the international search report

28 OCT 1994

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
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Washington, D.C. 20531Authorized officer
Alpus H. HSU
ALPUS H. HSU

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/04421

A. CLASSIFICATION OF SUBJECT MATTER: US CL :

U.S.CL.: 340/825.06, 825.5, 825.51; 348/390, 397, 399, 404; 370/79, 84, 85.6, 85.7, 95.1, 118

B. FIELDS SEARCHED

Minimum documentation searched

Classification System: U.S.

U.S.CL.: 340/825.06, 825.5, 825.51; 348/384, 385, 387, 388, 390, 397, 399, 403, 404, 405, 406, 423, 473, 474, 487;
370/60, 60.1, 62, 79, 84, 85.6, 85.7, 94.1, 94.2, 95.1, 112, 118